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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/650,719	05/20/1996	JEFFREY S. MAILLOUX	95-0653	2941

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EXAMINER
KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

	Application No.	**Applicant(s)**
Office Action Summary	08/650,719	MAILLOUX ET AL.
	Examiner	**Art Unit**
	Hong C Kim	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>*16 September 2002*</u> .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-9,33-35,46,48-50,59-61,63 and 64* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-9,33-35,46,48-50,59-61,63 and 64* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *37* .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

Detailed Action

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37

CFR 1.114. Applicant's submission filed on 9/16/02 has been entered.

2.   Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are presented for examination. This

office action is in response to the REC filed on 9/16/02.

3.   Receipt is acknowledged of information disclosure statement filed on 9/16/02, which the

statement has been placed of record in the file. Information disclosed and listed on PTO 1449

was considered.

4.   Applicant amended that this application is CIP of 08/584,600. However, application is

not entitled to the benefit of earlier filing date of 08/584,600 because claims are not supported by

the parent application. It also raises 112 first paragraph issue, because 35 U.S.C. 120 states that

"An application for patent for an invention disclosed in the manner provided by the first

paragraph of section 112 of this title in an application previously filed in the United States". In

other words, this application does not repeats a substantial portion of prior Application, see

H. Kim, WP6.1, 08 09 pm, November 25, 2002 Asynchronous memory with mode selection for burst or pipelined operation   10th Action

MPEP 201.08. Also application is not entitled to the benefit of earlier filing date of 08/584,600

because this application is to a different inventive entity and is commonly assigned with the

Patented prior application. Also it would raise an issue of double patenting since the this

application is to a different inventive entity and is commonly assigned with the Patented prior

application.

5.   It is noted that this application appears to claim subject matter disclosed in the co-pending

section or related section of this application. Applicants are reminded to maintain a clear line of

demarcation between this application and co-pending or related applications to avoid possible

double patenting (i.e U.S Pat. No 5966724).

DOUBLE-PATENTING

6.   The non-statutory double patenting rejection, whether of the obviousness-type or non-

obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy

reflected in the statute) so as to prevent the unjustified or improper timewise extension of the

"right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA

1969); *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum,* 686 F.2d 937,

214 USPQ 761 (CCPA 1982); *In re Longi,* 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In

re Goodman,* 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be

used to overcome an actual or provisional rejection based on a non-statutory double patenting

ground provided the conflicting application or patent is shown to be commonly owned with this

application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

7.   Claims 59-60 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claim 36 of copending Application

No. 08/984,563. Although the conflicting claims are not identical, they are not patentably

distinct from each other because both sets of claims are related to a method of accessing a storage

device, comprising: a first address, burst and pipelined mode, selecting inputting and outputting

information, selecting a burst mode and a pipelined mode, utilizing a second address to access

data in a memory. Both sets of claims recited similar inventive concept of accessing a memory

in burst and pipelined mode except: Claims 59-60 of the present invention comprises less

specific steps than as claimed in the Application No. 08/984,563. However, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to utilize teaching

of 08/984,563 and modify an external row address to a first address and a first external column

address to a second address of the copending application to arrive invention of the present

application.

8.   Claim 61 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 59 of copending Application No. 08/984,561. In view of Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device in burst and pipelined mode. Claims 61 of the present invention comprises less comprises less elements than as claimed in the Application No. 08/984,563. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to delete additional limitations of maintaining a first enabling signal in an active state of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

9.   Claim 61 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

It appears that "selecting a pipeline mode of operation; proving a new external address for every

associated with --- while in a burst mode of operation; providing an initial external address

associated --- in the pipelined mode of operation; and while in the burst mode of operation,

generating at least one subsequent internal address patterned after the initial external address

provided while in the pipelined mode of operation" was not described in the specification, at the

time the application was filed. In other words, although the specification (pg.27, 1-11; pg.38,

line 11-15; and pg. 39, lines 9-16) discribes burst and pipeline operations, the specification does

not specifially discribe claimed limitation of "while in the burst mode of operation, generating at

least one subsequent internal address patterned after the initial external address provided while in

the pipelined mode of operation".

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e)   the invention was described in a patent granted on an application for patent by
> another filed in the United States before the invention thereof by the applicant for patent,
> or on an international application by another who has fulfilled the requirements of
> paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by
> the applicant for patent.

11.   Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are rejected under 35 USC 102(e) as

being anticipated by _Manning, U.S. Patent 5,610,864_.

As to claim 1, *Manning* discloses the invention as claimed. *Manning* discloses an

asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchrous memory, col.

col. 6 lines 14-16) comprising mode circuitry to select between a burst mode (col. 6 lines 14-34

and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "the current invention include a

pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst

mode" read on this limitation, in other words, in order to work in the pipeline architecture one

has to select pipeline mode); and circuitry operable in either the burst mode or the pipelined

mode coupled to the mode selection circuity and configure to select between two modes.(Fig. 1

Ref. 40 and col. 6 lines 14-16 & col. 5 lines 41-50).

As to claim 50, Manning further discloses a microprocessor (Fig. 11 Ref. 112). Manning

also disclose a system clock (col. 8 line 46) in the microprocessor to operate the processor.

As to claim 2, Manning further discloses the burst mode and the pipelined mode are EDO

modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 3, Manning further discloses the pipelined mode is an EDO mode (col. 5

lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 4, Manning further discloses the burst mode is and EDO mode (col. 6 line

15).

As to claim 5, <u>Manning</u> further discloses the mode circuitry includes a buffer, the buffer

for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 6, <u>Manning</u> further discloses the mode circuitry includes at least one counter

for incrementing the address (Fig. 1 Ref. 26 and col 5 lines 51-62).

As to claim 7, <u>Manning</u> further discloses the mode circuitry includes receiving an

external address (Fig. 1 Ref. 16 and col. 4 lines 16-28).

As to claim 8, <u>Manning</u> further discloses the mode circuitry includes a buffer, the buffer

for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 9, <u>Manning</u> further discloses the mode circuitry includes multiplexed device

for providing an internally generated address to the storage device (Fig. 1 Refs. 26 and 30 and

col. 5 lines 51-62 & col. 3 lines 20-23, selection of external or internal address reads on this

limitation).

As to claims 33, 59, and 60, *Manning* discloses a method for accessing a storage device

(Fig. 1), comprising: receiving a first address to the storage device (Fig. 2 ROW); selecting

between an asynchronously accessible (Fig. 1 and EDO constitutes asynchrous operation, col.

col. 6 lines 14-16) burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode

(col. 5 lines 43-50) of operations of the storage device; selecting between outputting information

from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations

read on this limitation); obtaining a second address to the storage device (Fig. 2 /COL), and

asynchronously accessing a storage element of the storage device in the selected mode of

operation using the first address and the second addresses (Fig. 2, DQ and col. 5 lines 41-50, col.

6 lines 14-26 & col. 7 lines 43-54).

As to claim 34, Manning further discloses a step of switching between the pipelined

mode and burst mode (col. 5 lines 41-50, col. 6 lines 14-16 and col. 5 lines 42-50).

As to claim 35, Manning further discloses the second address is an external address (Fig.

1 Refs 16 and 30 and col. 4 lines 16-28).

As to claim 46, *Manning* discloses a method for accessing several different locations in

an asynchronously a storage device (Fig. 1 and EDO constitutes asynchrous operation, col. col. 6

lines 14-16), comprising: selecting a pipelined mode of operation (col. 5 lines 42-50); providing

a new external addresses for every access associated with accessing the asynchronously-

accessible memory device while in the pipelined mode of operation (col. 5 lines 42-50, "where

memory accesses are performed sequentially" and "one access per cycle" read on this limitation);

switching a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 43-54); providing an

initial external address associated with asynchronously accessing the asynchronously-accessible

memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and

generating at least one subsequent internal address patterned after the initial external address

while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67).

As to claims 48 and 49, Manning further discloses column, row, application, fixed access

based switching (col. 5 line 42 thru col. 6 line 34) for the burst mode and the pipelined mode.

As to claim 61, *Manning* discloses a method for accessing several different locations in

an asynchronously a storage device (Fig. 1 and EDO constitutes asynchrous operation, col. col. 6

lines 14-16), comprising: selecting a pipelined mode of operation (col. 5 lines 42-50); providing

a new external addresses for every access associated with accessing the asynchronously-

accessible memory device while in the pipelined mode of operation (col. 5 lines 42-50, definition

of the pipeline "where memory accesses are performed sequentially" and "one access per cycle"

reads on this limitation); switching a burst mode of operation (col. 6 lines 14-34 and col. 7 lines

43-54); providing an initial external address associated with asynchronously accessing the

asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and

col. 8 line 67); and generating at least one subsequent internal address patterned after the initial

external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67).

As to claim 63, *Manning* discloses a storage device, comprising; an array of memory cells

(col. 4 lines 13-15); mode circuitry for receiving a burst/pipeline signal (col. 5 lines 41-50, col. 6

lines 14-34 & col. 7 lines 43-54); and operation circuitry operable in a burst or a pipeline mode

of operation depending upon the burst/pipeline signal, the operation circuitry switchable between

burst and pipeline modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 43-

54).

As to claim 64, *Manning* discloses a memory circuit, comprising; an array of memory

cells (col. 4 lines 13-15); burst/pipeline selection circuitry for determining a burst or a pipeline

mode of operation of the memory circuit (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 43-

54); and mode circuitry capable of operation in either a burst mode or a pipeline mode of

operation, and switchable between burst and pipeline modes of operation (col. 5 lines 41-50,

col. 6 lines 14-34, and col. 7 lines 43-54).

Response to Amendment

12.   Applicant's arguments filed on 9/16/02 have been fully considered but they are not

persuasive.

Applicant's argument on page 4 that the reference does not disclose selecting between a

burst mode and a pipeline modes of operations is not considered persuasive.

"The current invention include a pipelined architecture" (col. 5 lines 43-49 in Manning) and

"switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16

& Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation, in other words, in order to

work in the pipeline architecture one has to select pipeline mode. Also given the teachings of

above reference one of the ordinary skill in the art at the time the invention was made would have

been lead to an obvious fashion to provide a pipelined page mode circuitry since Manning

discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which

would increase accessing speed.

Therefore, broadly written claims are disclose by the references cited.

In response to applicant's argument that the references fail to show certain features of

applicant's invention, it is noted that the features upon which applicant relies (i.e., enabling

switching between pipeline or burst operations with in the same memory, "on-the-fly") are not

recited in the rejected claim(s). Although the claims are interpreted in light of the specification,

limitations from the specification are not read into the claims. See *In re Van Geuns*, 988

F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

14.   a shortened statutory period for response to this action is set to expire 3 (three) months

and 0 (zero) days from the mail date of this letter. Failure to respond within the period for

response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02,

710.02(b)).

15.   Applicants are requested to number each line of each <u>claim</u> starting with line number one

to provide easier communication in the future.

16.   When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the art

disclosed by the references cited or the objections made. He or she must also show how the

amendments avoid such references or objections.   See 37 C.F.R. § 1.111(c).

17.   When responding to the office action, Applicants are advised to provide the examiner

with the line numbers and page numbers in the application and/or references cited to assist

examiner to locate the appropriate paragraphs.

18.   Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The

Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703) 305-3900.

19.   **Any response to this action should be mailed to:**

> Commissioner of Patents and Trademarks
> Washington, D.C. 20231

> **or faxed to TC-2100:**
> After-final   (703) 746-7238
> Official   (703) 746-7239 (for formal communications intended for

entry)

> Non-Official/Draft (703) 746-7240 (for informal or draft communications, please
label "PROPOSED" or "DRAFT")

> Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal
> Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
November 25, 2002